

Modulator for pager setup (TX) pre-alpha

- Options

- Square

- 555 timer

- Logic gate oscillator

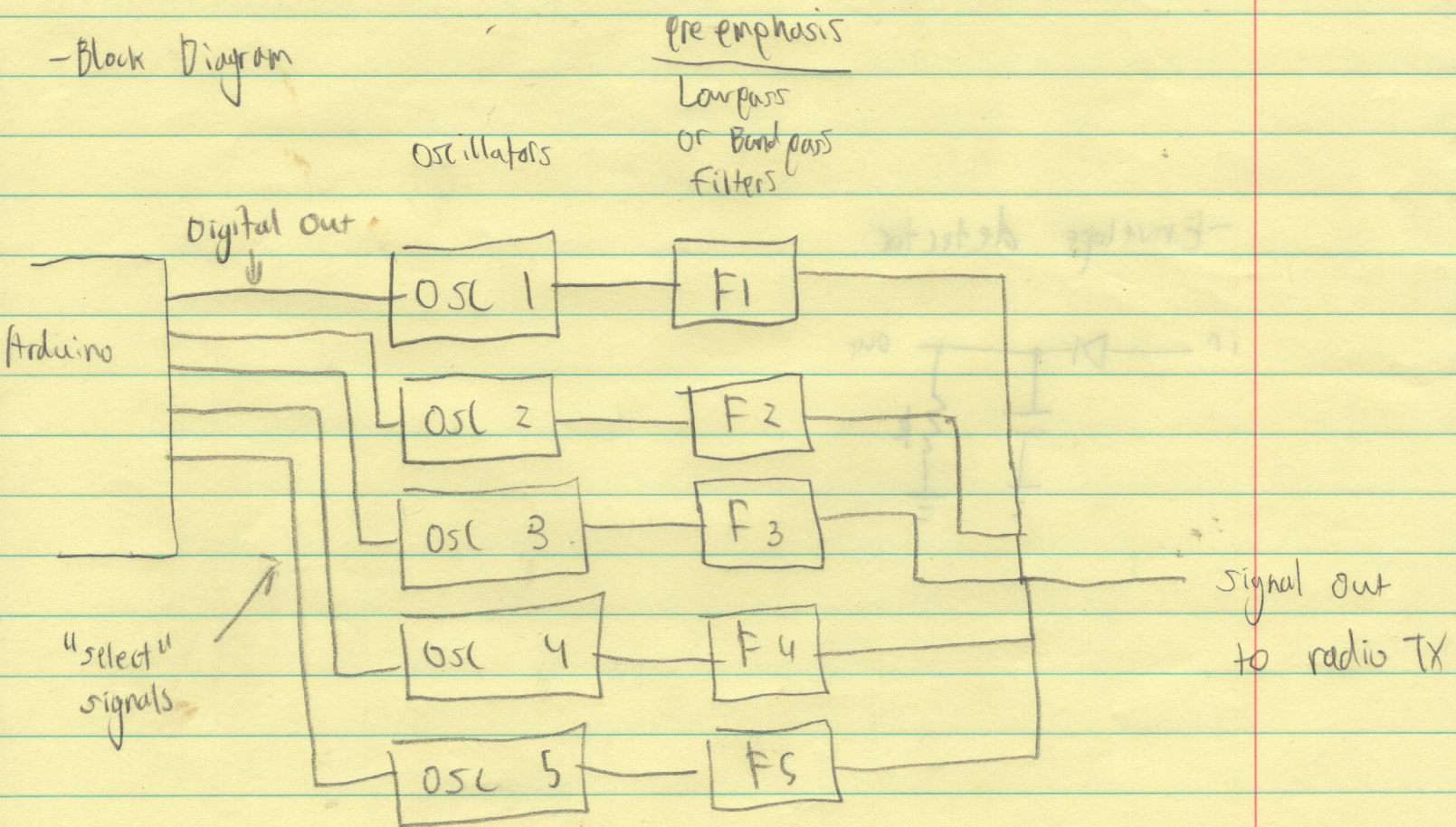
- 4046B voltage controlled square wave

- Sine

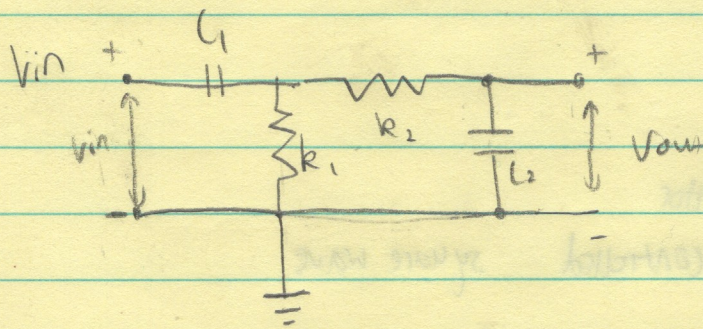
- Wien Bridge

- Phase shift

- Block Diagram



Band Pass filter for pager project

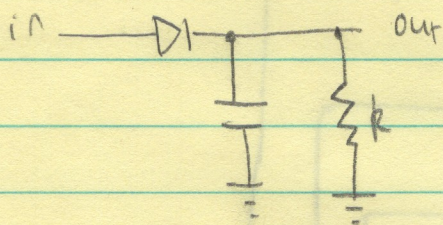


$$R_1 = R_2 = 10k\Omega$$

$$C_1 = \frac{1}{2\pi f_c R}$$

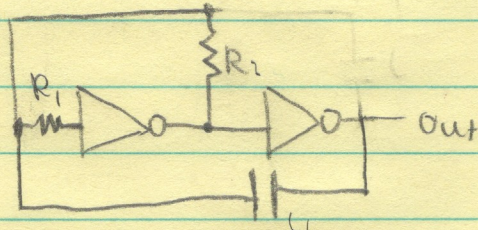
$$C_2 = \frac{1}{2\pi f_c R}$$

-Envelope detector



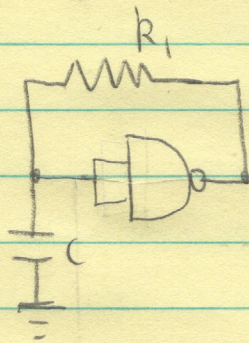
Astable Multivibrator

- Using NOT gates (CMOS including 4069)



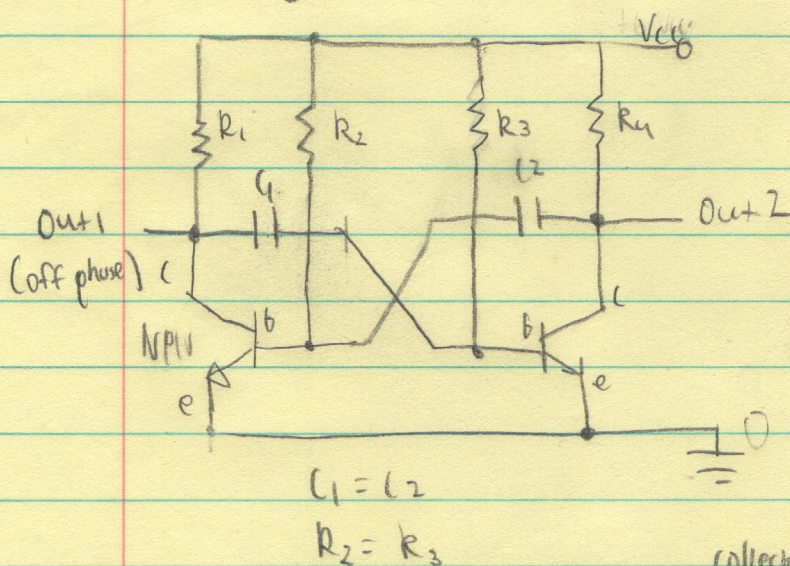
$$F = \frac{1}{2.2 R_2 C_1}$$

- Using NAND gates configured as NOT gates



(may configure as current sink to make HIGH when out is low and tied to ground)

- Using two NPN transistors



0.69 time constant

$$\text{Period } (T) = t_1 + t_2$$

$$t_1 = 0.69 C_1 R_3$$

$$t_2 = 0.69 C_2 R_2$$

$$\text{freq. } (f) = \frac{1}{T} = \frac{1}{1.38 RC}$$

$$C_1 = C_2$$

$$R_2 = R_3$$

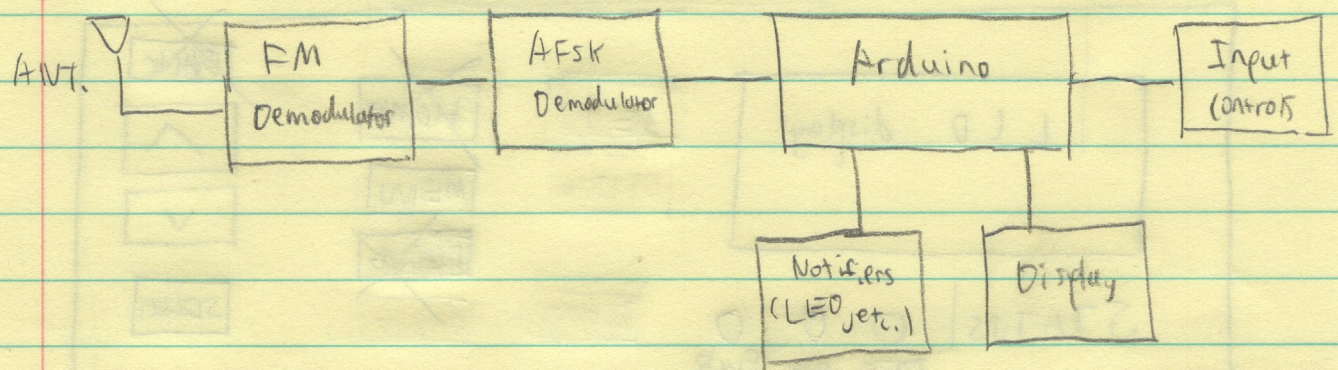
$$R_1 = R_4 = V / I_c$$

$$2N2222 \quad I_c = 600 \text{ mA}$$

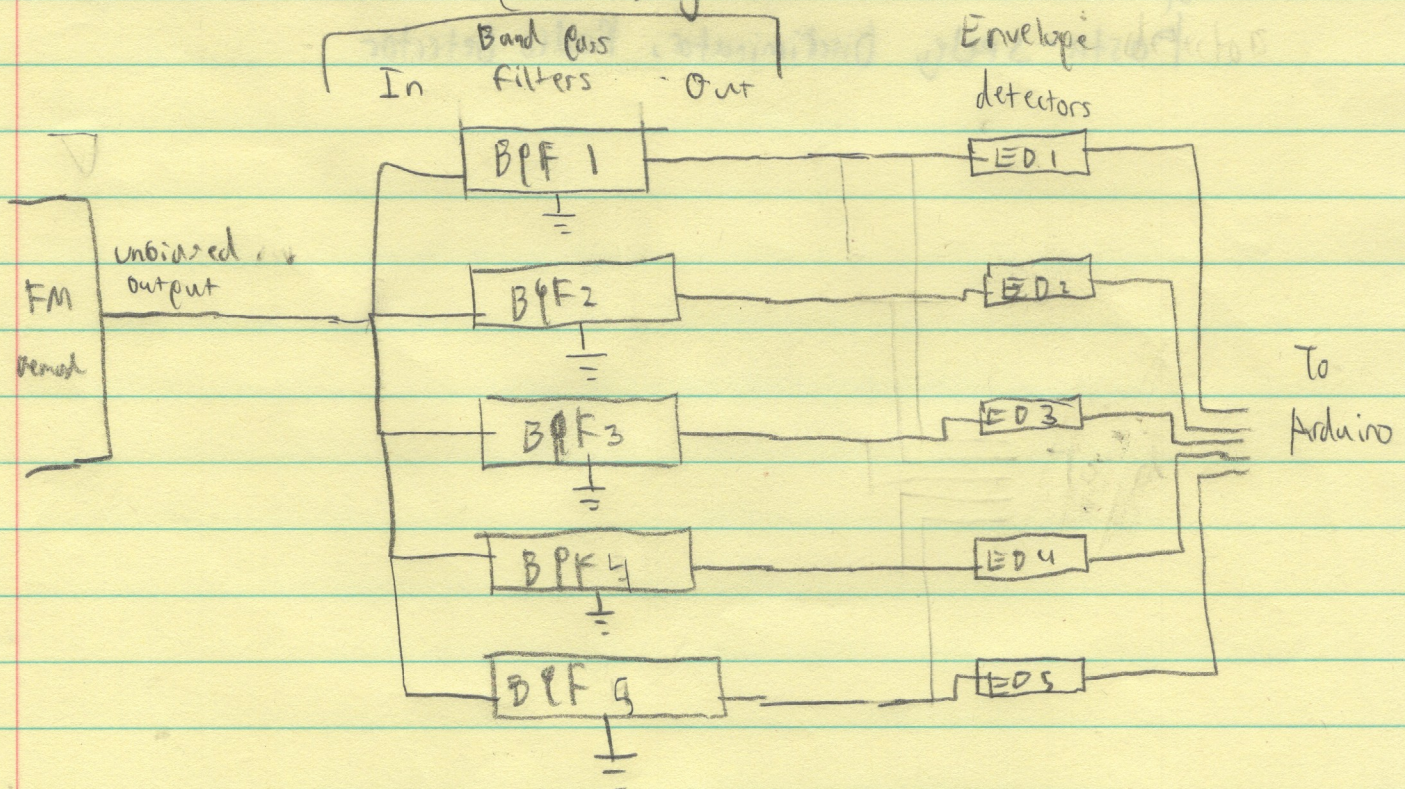
collector current

Open Pager Project hardware design pre-alpha

- Block Diagram (High level)



- AFSK Demodulator (block diagram)



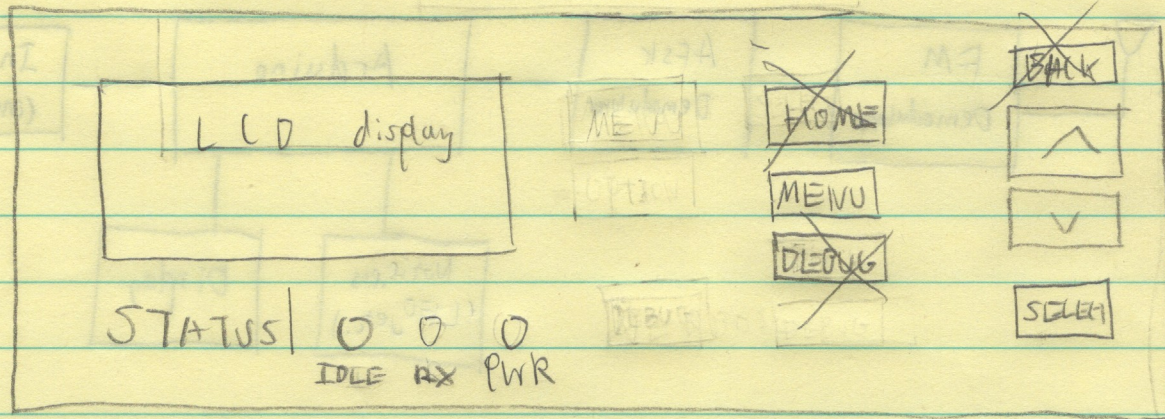
~~OPP~~ User interface

pre-alpha

- Interface Overview

- Diagram

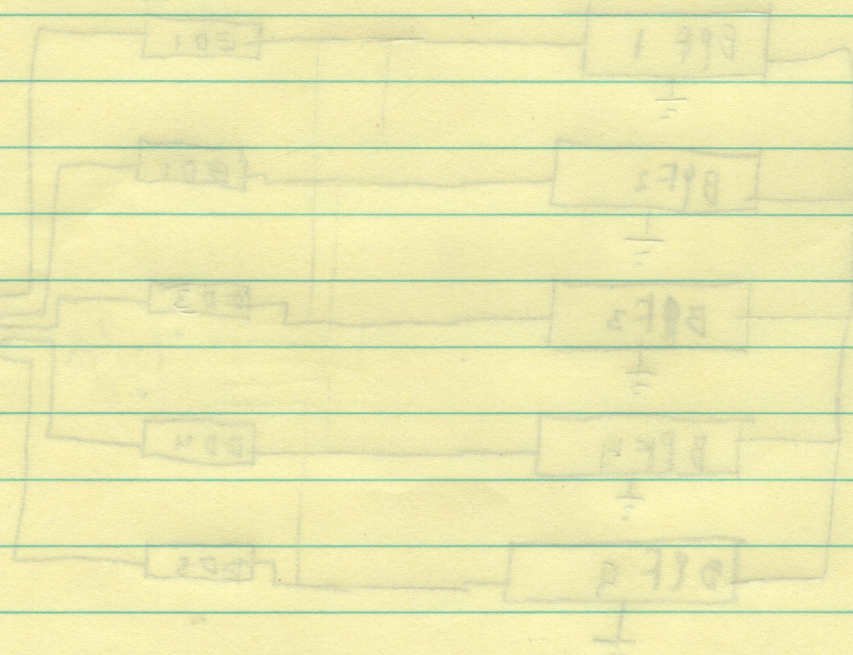
• Not final form factor



- FM Demodulation

- Type of detector

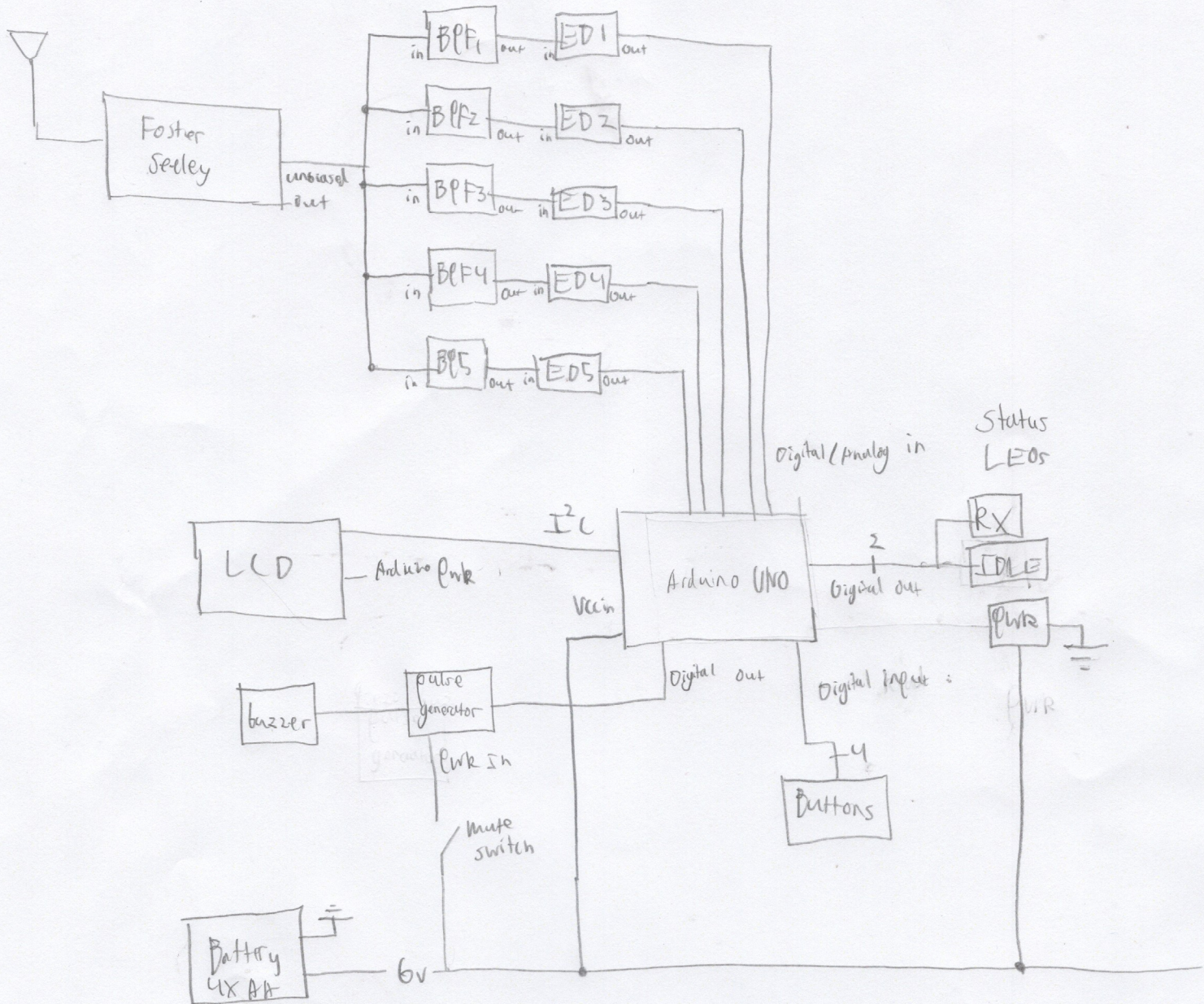
Foster-seeley Discriminator, Radio Detector



Pager block diagram

pre-alpha

FM in FM Demod Analog In Digital out



Open Pager Project Trials pre-alpha

- NOT gate Astable multivibrator Functional

- Preliminary test ($\sim 500 \text{ Hz}$)

$V_{CC} = 9V$
 $R_1 = 100k$

$$F = \frac{1}{2.2 R_2 C_1}$$

$R_2 = 10k$ $F = \sim 500 \text{ Hz}$

$$500 = \frac{1}{2.2(10,000) C_1}$$

Reality: $C_1 = 70 \text{ nF}$

$R_1 = 100k$

result $R_2 = 10.01k$

$$F = 736 \text{ Hz}$$

$$11 \cdot 10^6 \text{ Hz} \cdot \Omega = \frac{1}{C_1}$$

$$C_1 = 9.09 \cdot 10^{-8} \text{ F} \left(\frac{1}{\text{Hz} \cdot \Omega} \right)$$

$$= 90.9 \text{ nF (Theoretical)}$$

- 2N2222 Astable Multivibrator

- Trial 1 ($\sim 500 \text{ Hz}$)

$V_{CC} = 9V$ actual $\sim 9.3V$

$V_{CE} = IR$

Collector current = 600 mA

$$R_1 = R_2 = \frac{9}{600 \cdot 10^{-3}} = 15 \Omega$$

Reality: $C_1 = C_2 = 110.4 \text{ nF}$

$$500 = \frac{1}{1.38 k \Omega} = F$$

$R_2 = R_3 = 100k$

$$500 = \frac{1}{1.38(100,000) C}$$

$R_1 = R_4 = 20 \Omega$

$$F = \sim 724 \text{ Hz}$$

$$69 \cdot 10^6 = \frac{1}{C} \quad C = 1.45 \cdot 10^{-8} \text{ F} = 14.5 \text{ nF}$$

- Notes

'much louder output compared to NOT gate



- Trial 2

$$500 = \frac{1}{1.38(100,000) C_1} = 1.45 \cdot 10^{-6} \text{ F} \quad 1.45 \mu\text{F}$$

$R_1 = 100k = R_2 \quad C_1 = 1 \mu\text{F}$